Amendments to the Claims:

Please amend claims 1-14, 16, and 17.
Please delete claims 15 and 18 as follows.

1. (Currently amended) An apparatus for generating a supply voltage internally within an integrated circuit comprising:

a charge pump stage structure having a pumping capacitor connected to a pumping node, a first PMOS device connected ~~to~~ between an input node and said pumping node, said first PMOS device configured to electrically communicate with said pumping capacitor, wherein said first PMOS device is configured to connect said pumping node to said input node when said pumping capacitor is not boosted;

a second PMOS device connected ~~to~~ between an output node and said pumping node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output node when said pumping capacitor is boosted, said second PMOS device having a gate terminal connected to a pumping node of another charge pump stage structure of a symmetrical charge pump, wherein said second PMOS device is configured to prevent reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said ~~second~~ first PMOS device to prevent ~~said~~ current feedback from said pumping node to said input node.

2. (Currently amended) The apparatus of claim 1, wherein said third PMOS device is configured to connect the ~~pump~~ pumping node to a gate terminal of said ~~second~~ first PMOS device in order to prevent said current feedback from said pumping node to said input node when said pumping capacitor is boosted.

3. (Currently amended) The apparatus of claim 1 further including:

an auxiliary capacitor connected to a gate terminal of said first PMOS device, wherein said auxiliary capacitor is configured to generate an undershoot on said gate of said first PMOS device, and wherein said auxiliary capacitor is configured to switch said ~~apparatus~~ first PMOS device to an "ON" state when an electrical current is transferred from said input node to said pumping node.

4. (Currently amended) An apparatus for generating a supply voltage internally within an integrated circuit comprising:

a symmetrical charge pump stage structure comprising a first substructure and a second substructure, each of said ~~substructure~~ substructures having a pumping capacitor connected to a pumping node, a first PMOS device connected ~~to~~ between an input node and said pumping node, said first PMOS device configured to electrically communicate with said ~~coupling~~ pumping capacitor; wherein said first PMOS device is configured to connect said pumping node to said input node when said pumping capacitor is not boosted;

each of said substructures having a second PMOS device connected [to] between an output node and said pumping node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output node when said pumping

capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output node to said pumping node when said pumping capacitor is not boosted, said second PMOS device having a gate terminal connected to a pumping node of the other substructure, wherein said second PMOS device is configured to prevent a reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

each of said substructures having a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said ~~second~~ first PMOS device to prevent ~~a reversal~~ the reverse current feedback from said pumping node to said input node when said pumping capacitor is boosted.

5. (Currently amended) The apparatus of claim 4, wherein said third PMOS device is configured to switch ~~a~~ the gate terminal of said first PMOS device to a boosted pump node potential in order to prevent said reverse current feedback from said pumping node to said input node when said pumping capacitor is boosted.

6. (Currently Amended) The apparatus of claim 4, wherein each ~~of~~ said ~~substructure~~ substructures further comprises:

an auxiliary capacitor connected to a gate terminal of said first PMOS device, wherein said auxiliary capacitor is configured to generate an undershoot on said gate of said first PMOS device, and wherein said auxiliary capacitor is configured to switch said ~~apparatus~~ first PMOS device to an "ON" state when an electrical current is transferred from said input node to said pumping node.

7. (Currently Amended) An apparatus for generating a supply voltage internally within an integrated circuit comprising:

an independently controlled charge pump stage having an input control node, a pumping capacitor connected to a pumping node, a first PMOS device connected ~~to~~ between said input control node and said pumping node, said first PMOS device configured to electrically communicate with said ~~coupling~~ pumping capacitor, wherein said first PMOS device is configured to connect said pumping node to said input control node when said pumping capacitor is not boosted;

a second PMOS device connected ~~to~~ between an output control node and said pumping node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output control node when said pumping capacitor is boosted, said second PMOS device configured to prevent ~~a reversal~~ reverse current feedback from said output control node to said pumping node when said pumping capacitor is not boosted, said second PMOS device having a gate terminal connected to a pumping node of another charge pump stage of a symmetrical charge pump, wherein said second PMOS device is configured to prevent a reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device electrically communicating with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said ~~second~~ first PMOS device to prevent ~~a reversal~~ reverse current feedback from said pumping node to said input control node when said pumping capacitor is boosted; wherein said third PMOS device has a gate terminal at which is provided a control signal for independently controlling said third PMOS device.

8. (Currently Amended) The apparatus of claim 7, wherein said third PMOS device is configured to switch a gate of said first PMOS device to a boosted pump node potential in order to prevent said reverse current feedback from said pumping node to said input control node when said pumping capacitor is boosted.

9. (Currently Amended) The apparatus of claim 7, ~~wherein each said substructure further comprises~~ further including:

an auxiliary capacitor connected to a gate terminal of said first PMOS device, wherein said auxiliary capacitor is configured to generate an undershoot on said gate of said first PMOS device, and wherein said auxiliary capacitor is configured to switch said ~~apparatus~~ first PMOS device to an "ON" state when an electrical current is transferred from said input control node to said pumping node.

10. (Currently Amended) An apparatus for generating a supply voltage internally within an integrated circuit comprising:

an independently controlled symmetrical charge pump stage structure comprising a first independently controlled substructure and a second independently controlled substructure, each of said independently controlled ~~substructure~~ substructures having:

an input control node;

a pumping capacitor connected to a pumping node;

a first PMOS device connected to said input control node, said first PMOS device configured to electrically communicate with said ~~coupling~~ pumping capacitor, wherein said first PMOS device is configured to connect said pumping node to said input control node when said pumping capacitor is not boosted;

a second PMOS device connected ~~to~~ between an output control node; said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical current from said pumping node to said output control node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output control node to said pumping node when said pumping capacitor is not boosted, said second PMOS device having a gate terminal connected to a pumping node of the other substructure, wherein said second PMOS device is configured to prevent reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said ~~second~~ first PMOS device to prevent ~~a reversal~~ reverse current feedback from said pumping node to said input control node when said pumping capacitor is boosted; wherein said third PMOS device has a gate terminal at which is provided a control signal for independently controlling said third PMOS device.

11. (Currently Amended) The apparatus of claim 10, wherein said third PMOS device is configured to switch a gate of said first PMOS device to a boosted pump node potential in order to prevent said reverse current feedback from said pumping node to said input control node when said pumping capacitor is boosted.

12. (Currently Amended) The apparatus of claim 10, wherein each of said independently controlled ~~substructure~~ substructures further comprises:

an auxiliary capacitor connected to said first PMOS device, wherein said auxiliary capacitor is configured to generate an undershoot on said gate of said first PMOS device, and wherein said auxiliary capacitor is configured to switch said ~~apparatus~~ first PMOS device to an "ON" state when an electrical current is transferred from said input control node to said pumping node.

13. (Currently Amended) An apparatus for generating a supply voltage internally within an integrated circuit comprising:

a plurality of symmetrical charge pump stages cascade-connected in series having:

a first symmetrical pump charge stage connected to an input node; ~~and~~

a last symmetrical pump charge stage connected to an output node; and

wherein each of said symmetrical pump charge stages further comprises a first substructure and a second substructure, each of said first and second substructures further comprises:

a pumping capacitor connected to a pumping node;

a first PMOS device connected between an input node and said pumping node, said first PMOS device configured to electrically communicate with said coupling capacitor, wherein said first PMOS device is configured to connect said pumping node to said input node when said pumping capacitor is not boosted;

a second PMOS device connected between an output node and said pumping node; said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer

electrical charge from said pumping node to said output node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output node to said pumping node when said pumping capacitor is not boosted, said second PMOS device having a gate terminal connected to a pumping node of another charge pump stage structure of a symmetrical charge pump, wherein said second PMOS device is configured to prevent reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said first PMOS device to prevent the reverse current feedback from said pumping node to said input node when said pumping capacitor is boosted.

14. (Currently Amended) The apparatus of claim 13 further comprising;

at least one intermediate symmetrical pump charge stage ~~therebetween~~ between the first symmetrical pump charge stage connected to the input node and the last symmetrical pump charge stage connected to the output node.

15. (Cancelled)

16. (Currently Amended) An apparatus for generating a supply voltage internally within an integrated circuit comprising:

a symmetrical pump charge stage connected to an input node; and

a plurality of independently controlled symmetrical charge pump stages cascade-connected in series comprising:

a first independently controlled symmetrical pump charge stage connected to said symmetrical pump charge stage; and

a last independently controlled symmetrical pump charge stage connected to an output node;

wherein each of said independently controlled symmetrical charge stages further comprises a first independently controlled substructure and a second independently controlled substructure, each said independently controlled substructure having:

an input control node;

a pumping capacitor connected to a pumping node;

a first PMOS device connected between said input control node and said pumping node, said first PMOS device configured to electrically communicate with said pumping capacitor, wherein said first PMOS device is configured to connect said pumping node to said input control node when said pumping capacitor is not boosted;

a second PMOS device connected between an output control node and said pumping node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical current from said pumping node to said output control node when said pumping capacitor is boosted, said second PMOS device configured to prevent reverse current feedback from said output control node to said pumping node when said pumping capacitor is not boosted; said second PMOS

device having a gate terminal connected to a pumping node of another charge pump stage of a symmetrical charge pump, wherein said second PMOS device is configured to prevent a reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said second device to prevent the reversal current feedback from said pumping node to said input control node when said pumping capacitor is boosted; wherein said third PMOS device has a gate terminal at which is provided a control signal for independently controlling said third PMOS device.

17. (Currently Amended) The apparatus of claim 16 further comprising:

at least one intermediate independently controlled symmetrical pump charge stage ~~therebetween~~ between the first symmetrical pump charge stage connected to the input node and the last symmetrical pump charge stage connected to the output node.

18. (Cancelled)